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Comparative Study of Atomic-Layer-Deposited Stacked (HfO_2/Al_2O_3) and Nanolaminated ($HfAlO_x$) Dielectrics on $In_{0.53}Ga_{0.47}As$

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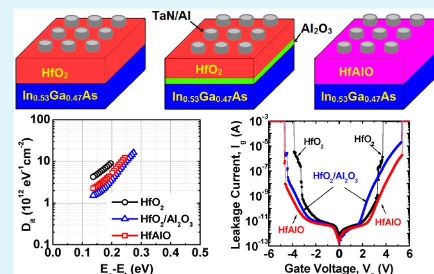
Supporting Information

ABSTRACT: The high-k gate dielectric structures in stacked (HfO_2/Al_2O_3) and nanolaminated ($HfAlO_x$) forms with a similar apparent accumulation capacitance were atomic-layer-deposited on n-type $In_{0.53}Ga_{0.47}As$ substrates, and their electrical properties were investigated in comparison with a single-layered HfO_2 film. Al-oxide interface passivation in both forms proved to be effective in preventing a significant In incorporation in the high-*k* film and reducing the interface state density. The measured valence band spectra in combination with the reflection electron energy loss spectra were used to extract the energy band parameters of various dielectric structures on $In_{0.53}Ga_{0.47}As$. A further decrease in the interface state density was achieved in the stacked structure than in the nanolaminated structure. However, in terms of the other electrical properties, the nanolaminated sample exhibited better characteristics than the stacked sample, with a smaller border trap density and lower leakage current under substrate injection conditions with and without voltage stressing.



KEYWORDS: *HfO_2, Al_2O_3, stacked structure, nanolaminated structure, $In_{0.53}Ga_{0.47}As$, atomic layer deposition*

1. INTRODUCTION

Recent research on III−V substrate-based metal-oxide-semiconductor field-effect transistors (MOSFETs) has been directed into gate stack and interface engineering, which has demonstrated promising results using various high-*k* dielectric films synthesized by atomic layer deposition (ALD).[1] The ALD process has several advantages over other deposition techniques such as sputtering and metal−organic (MO) chemical vapor deposition, in attaining high-*k* films with exceptionally high dielectric quality as well as accurate thickness controllability.[2] In particular, one of the most unique capabilities is the MO precursor-incurred self-cleaning effect, which entails in situ reduction of the interface oxide layer[3,4] and facile manipulation of gate dielectric engineering with various high-*k* materials enabled by a submonolayer deposition rate.

ALD-HfO_2 film on III−V compound substrates has attracted great interest due to its higher dielectric constant than Al_2O_3 film, which makes it suitable for further scaling-down of devices. However, using a single-layered HfO_2 film has raised several problems, such as poor interface quality, poor thermal stability, and large hysteresis.[5−7] Recently, gate dielectric engineering was successfully adopted in high-*k*/III−V compound semiconductor technology by exploiting the advantages of each of the dielectric films, including the outstanding interface quality of Al_2O_3 and the high dielectric constant of HfO_2, in the form of stacked (HfO_2/Al_2O_3) or nanolaminated ($HfAlO_x$) structures.[8−15] However, direct comparison of these dielectric structures on an $In_xGa_{1-x}As$ substrate, the most promising candidate for n-channel MOSFETs, in terms of interface and electrical characteristics such as stability under electrical stressing, has been quite rare.

In this work, stacked and nanolaminated dielectric structures with a similar accumulation capacitance were grown in situ on $In_{0.53}Ga_{0.47}As$ substrates by ALD and compared with a single-layered HfO_2 film as a reference sample. The energy band parameters of various dielectric structures were evaluated, and various electrical characterizations regarding capacitance−voltage (C−V), leakage current−voltage (I−V), and electrical stability behavior under different stressing conditions were conducted.

2. EXPERIMENTAL SECTION

N-type $In_{0.53}Ga_{0.47}As$ (Si-doped with a concentration of 1×10^{17} cm^{-3}) epitaxially grown on InP was used as a substrate for this experiment. After sequential surface cleaning with ∼1% HF and ∼21% $(NH_4)_2S$ solutions at room temperature for 4 and 10 min, respectively,[16] the samples were loaded into an ALD system within 5 min after cleaning (**Caution:** HF is extremely corrosive and $(NH_4)_2S$ is also toxic. They must be handled with extreme care.) For the ALD process of Hf- and Al-oxide films, tetrakis(ethylmethylamino)hafnium, trimethylaluminum, H_2O, and N_2 were used as the Hf-precursor, Al-precursor, oxidant, and purging gas, respectively. The processes were conducted at a deposition temperature of 300 °C. Three gate dielectric structures with a total thickness of ∼7 nm were prepared for comparative study: HfO_2/Al_2O_3 and $HfAlO_x$ (HfAlO) samples, in addition to HfO_2 as a reference sample. For the stacked HfO_2/Al_2O_3

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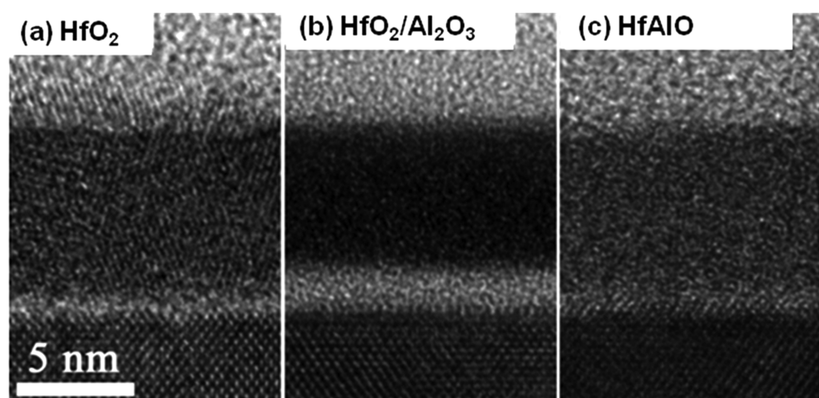

Figure 1. HRTEM images of as-deposited (a) HfO_2, (b) HfO_2/Al_2O_3, and (c) HfAlO dielectric structures on $In_{0.53}Ga_{0.47}As$ substrates. All of the dielectric structures were confirmed to have a similar total physical thickness of ∼7 nm.

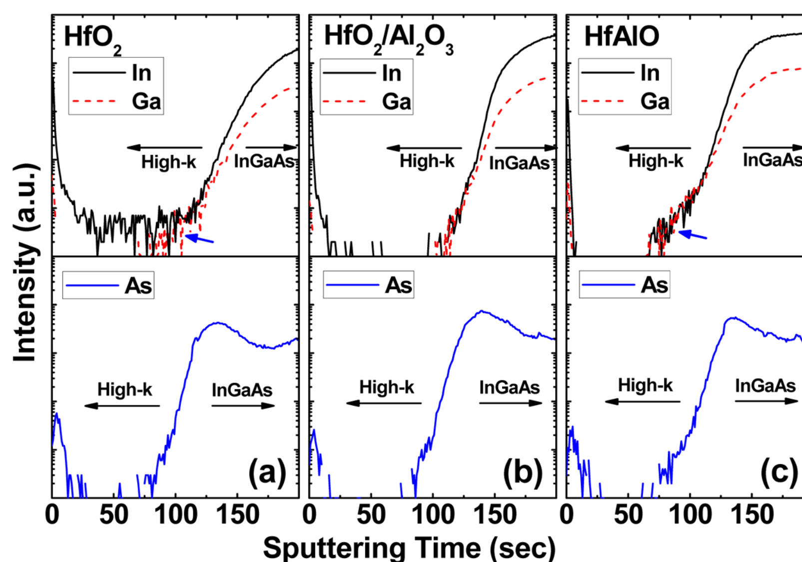

Figure 2. ToF-SIMS depth profiles of In, Ga, and As elements in (a) HfO_2, (b) HfO_2/Al_2O_3, and (c) HfAlO films on $In_{0.53}Ga_{0.47}As$. The samples were annealed at 400 °C for 30 min in forming-gas ambient. The blue arrows indicate the diffusion of In and Ga atoms toward the high-*k* films.

sample, a ∼1.7-nm-thick Al_2O_3 film was first deposited as a passivation layer before the HfO_2 deposition. In the case of the HfAlO film, the ALD process started with an Al_2O_3 layer-forming step, and the relative Al atomic percentage with respect to Hf in the film was controlled to around 50%, which was verified by energy-dispersive X-ray spectroscopy measurement. The detailed ALD process parameters including the injection schedule and the number of ALD cycles are presented in Table S1 in the Supporting Information.

After the formation of various dielectric structures, the following characterizations were employed ex situ for comparative study. High-resolution transmission electron microscopy (HRTEM, JEOL JEM 2100F, and JEM ARM 200F) was used for both film thickness determination and microstructural characterization. The in-depth distribution of substrate elements (In, Ga, and As) in the high-*k* gate dielectric structures was measured by time-of-flight secondary ion mass spectroscopy (ToF-SIMS, ION-TOF TOF.SIMS 5). For the depth profiling of In and Ga atoms, O_2^+ sputtering and Bi^+ analysis guns were used in a dual-beam mode. On the other hand, Cs^+ sputtering and Bi^+ analysis guns were used for the As measurement. The band gap measurement of the dielectric films was conducted using reflection electron-energy-loss spectroscopy (REELS, VG ESCALAB-210) with an incident-electron energy of 1 keV. X-ray photoelectron spectroscopy (XPS, Kratos AXIS-NOVA) with a monochromatic Al Kα source (1486.7 eV) was employed for the valence band analysis. In order to examine the electrical properties, MOS capacitors were fabricated by patterning the sputter-deposited Al-capped TaN top electrode with an area of 7850 μm^2 via a lift-off technique, followed by forming-gas annealing at 400 °C for 30 min under a flow of 4% H_2/N_2 mixed gas. The electrical characterization was performed at room temperature in a shielded dark box. The C−V characteristics were measured at various frequencies ranging from 100 Hz to 1 MHz using an Agilent E4980A LCR meter. In addition, the leakage current characteristics with and without electrical stressing were measured using an Agilent B1500A semiconductor device analyzer.

3. RESULTS AND DISCUSSION

3.1. Film and Interface Characteristics. Figure 1 shows the cross-sectional HRTEM images of the as-deposited gate dielectric structures with a similar thickness of ∼7 nm formed on $In_{0.53}Ga_{0.47}As$ substrates. As can be seen in Figures 1(a) and 1(b), the polycrystalline HfO_2 single layer showed a minimal existence of the interfacial layer (IL), which was probably a couple of monolayers, and became mostly amorphous after introducing the ∼1.7-nm-thick Al_2O_3 passivation layer. The nanolaminated HfAlO sample also exhibited an amorphous state due to a large amount of Al incorporation.[17] The microstructural variation of the three different dielectric structures was further confirmed by the Fourier-transformed images of the dielectric regions in the HRTEM pictures, which can be found in Figure S1 in the Supporting Information. In

addition, HRTEM analysis was also performed on the MOS capacitor samples after forming-gas annealing at 400 °C for 30 min. Although the dielectrics underwent an additional postdeposition annealing step, their HRTEM images were almost identical to those of the as-deposited samples (see Figure S2 in the Supporting Information).

In order to examine the difference of the substrate-element distribution near the interface region with different high-*k* dielectric structures, ToF-SIMS depth profiling was performed, and its results are shown in Figure 2. For a direct comparison of the electrical characteristics, the samples were annealed identically to the MOS capacitor samples. As compared to the stacked and nanolaminated layers, a considerable amount of In diffusion toward the high-*k* film was observed when a single ALD-HfO_2 layer was used, showing a large amount of In incorporation (probably forming In-related oxides) even in the middle of the HfO_2 film. This could possibly be attributed to the existence of grain boundaries, which act as a fast diffusion path in the single ALD-HfO_2 film. Among the three samples, the stacked sample was the most effective in preventing the In out-diffusion and showed minimal existence near the interface region. In terms of the Ga distribution, both HfO_2 and nanolaminated samples exhibited some amount of Ga out-diffusion near the interface region, as compared to the stacked sample, which probably implies more abundance of the Ga-related oxides at the interfacial region. Meanwhile, in the case of As, all the samples exhibited similar depth profiles. These results elucidate that the introduction of the Al−O bonds at the interface region in either a stacked or a nanolaminated form can effectively prevent significant In out-diffusion, and, especially, the stacked form has minimal amounts of the In and Ga-oxides near the interface region.

For the HfO_2/Al_2O_3 stacked sample, it would not be possible to completely exclude the compositional intermixing at the interface region between HfO_2 and Al_2O_3. However, comparing the HRTEM images in Figures 1(b) and S2(b), no significant HRTEM-observable intermixing was identified, even after the postdeposition annealing at 400 °C. Hence, for the sake of simplicity, we assumed an ideal HfO_2/Al_2O_3 stacked structure with a negligible compositional intermixing for the band structure analysis. It was verified experimentally that the valence-band (VB) lineup of the heterostructure (HfO_2/Al_2O_3 on $In_{0.53}Ga_{0.47}As$ in our experiment) can be effectively estimated by the combination of the separately acquired VB spectra of the constituent materials.[18,19] Therefore, for the evaluation of the band structures of the samples prepared in this experiment, we used as-deposited single-layered HfO_2, Al_2O_3, and HfAlO films with a thickness of ~7 nm, excluding the HfO_2/Al_2O_3 stacked sample. Figures 3(a)−(c) compare the REELS spectra obtained from these samples. In the measured REELS spectra, a broad energy-loss peak originating from the plasmon excitation was found at around 15 eV for the HfO_2-containing samples, and 22 eV for the Al_2O_3-containing samples away from the elastic peak, which are consistent with the reported values of HfO_2 and Al_2O_3 films.[20] The band gap value of each dielectric was extracted from the gathered spectra by reading the onset point of the band-to-band excitation with an error range of ±0.05 eV. The intercepts of the linear extrapolation of the leading edge to the background level were ~5.65 eV, ~6.95 eV, and ~6.05 eV for the HfO_2, Al_2O_3, and HfAlO films, respectively. These values are very close to the reported values of the ALD-grown films[20,21] and show a

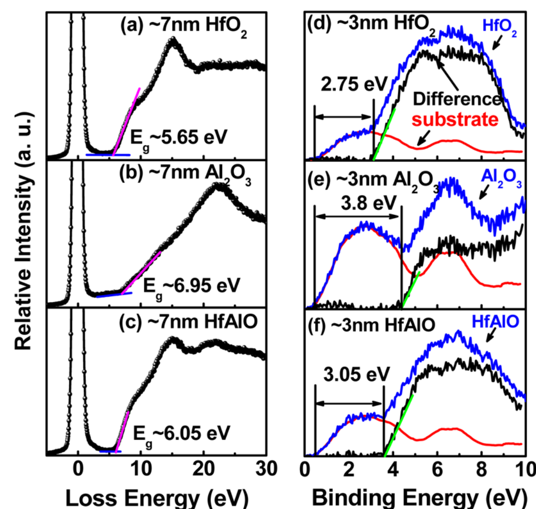

Figure 3. (a−c) REELS and (d−f) valence band spectra of various dielectric films on $In_{0.53}Ga_{0.47}As$: (a, d) HfO_2, (b, e) Al_2O_3, and (c, f) HfAlO.

systematic transition of the band gap as two pure dielectric films are mixed together.

Figures 3(d)−(f) show the VB spectra of the HfO_2, Al_2O_3, and HfAlO films. The VB offsets (VBOs) of the high-*k* films with respect to $In_{0.53}Ga_{0.47}As$ were obtained by subtracting the VB spectrum of the $In_{0.53}Ga_{0.47}As$ substrate from that of the high-$k/In_{0.53}Ga_{0.47}As$ structures as ~2.75 eV, ~3.8 eV, and ~3.05 eV for the HfO_2, Al_2O_3, and HfAlO films, respectively. Finally, the conduction band offset (CBO) was calculated by subtracting the measured VBO of the high-*k* on $In_{0.53}Ga_{0.47}As$ ($\Delta E_V^{High\text{-}k/InGaAs}$) and the band gap of the $In_{0.53}Ga_{0.47}As$ substrate (E_g^{InGaAs} = 0.75 eV) from the band gap of the high-*k* film ($E_g^{High\text{-}k}$):

$$\Delta E_C^{High\text{-}k/InGaAs} = E_g^{High\text{-}k} - \Delta E_V^{High\text{-}k/InGaAs} - E_g^{InGaAs} \quad (1)$$

By combining the band gap values and the VB lineup, the conduction band barrier height of the heterostructure can be determined. The extracted CBOs of the high-*k* films on $In_{0.53}Ga_{0.47}As$ ($\Delta E_C^{High\text{-}k/InGaAs}$) were ~2.15 eV, ~2.4 eV, and ~2.25 eV for the HfO_2, Al_2O_3, and HfAlO films, respectively. A stepwise increase was observed in E_g, ΔE_V, and ΔE_C for HfO_2, HfAlO, and Al_2O_3 films, respectively, on $In_{0.53}Ga_{0.47}As$, which is consistent with the previously reported result demonstrated on Si substrate.[22] By assuming that there is no significant interfacial mixing or thickness-dependence of the electronic structures, we have drawn schematic band diagrams of the single-layered (HfO_2), stacked (HfO_2/Al_2O_3), and nanolaminated (HfAlO) dielectric structures on $In_{0.53}Ga_{0.47}As$, which are shown in Figure 4.

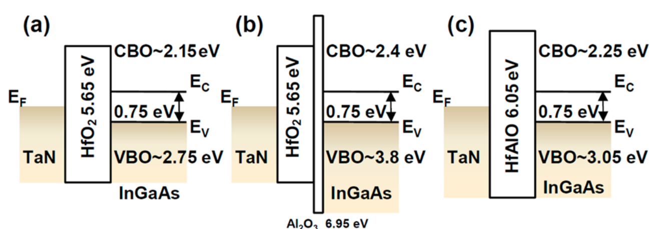

Figure 4. Schematic band diagrams of (a) $HfO_2/In_{0.53}Ga_{0.47}As$, (b) $HfO_2/Al_2O_3/In_{0.53}Ga_{0.47}As$, and (c) $HfAlO/In_{0.53}Ga_{0.47}As$ structures.

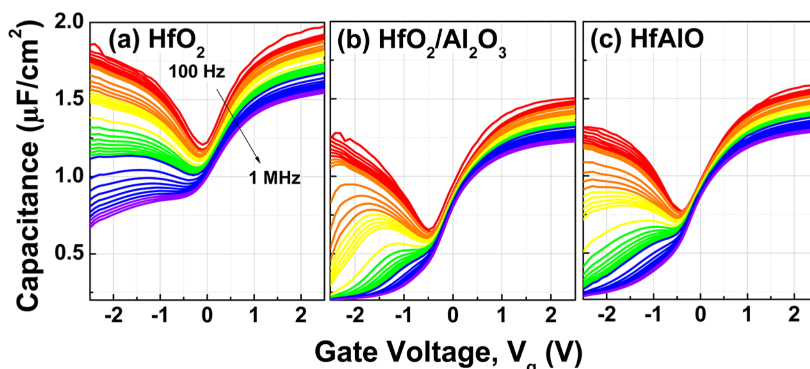

Figure 5. Multifrequency C−V characteristics of MOS capacitors made of (a) HfO_2, (b) HfO_2/Al_2O_3, and (c) HfAlO dielectric structures on $In_{0.53}Ga_{0.47}As$. 37 frequency responses ranging from 100 Hz to 1 MHz were recorded for each sample.

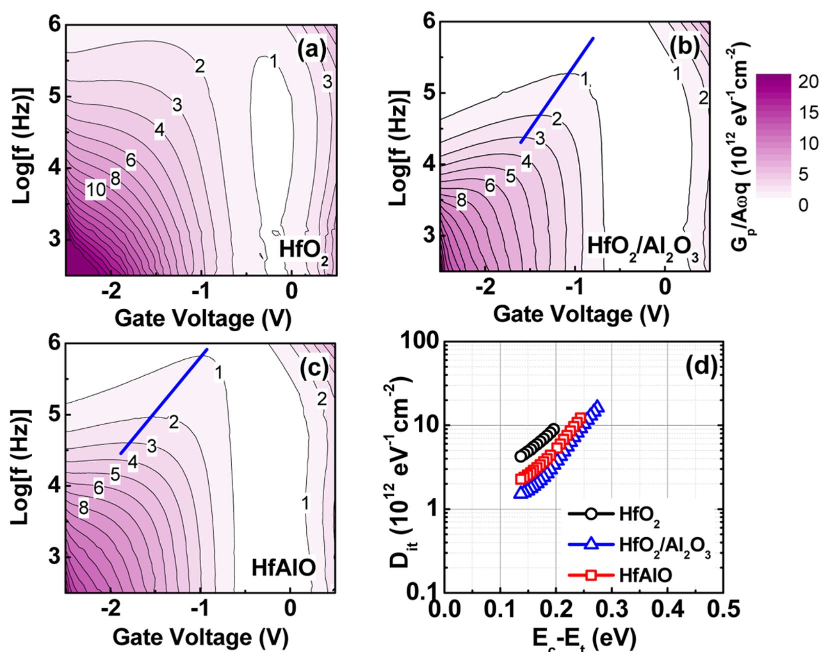

Figure 6. Normalized parallel conductance ($G_p/\omega qA$) as a function of gate voltage and measurement frequency for (a) HfO_2, (b) HfO_2/Al_2O_3, and (c) HfAlO gate dielectrics on $In_{0.53}Ga_{0.47}As$. The solid blue line indicates the approximate trace of $(G_p/\omega qA)_{max}$. (d) Interface trap distribution in the $In_{0.53}Ga_{0.47}As$ band gap obtained from the conductance measurement.

3.2. Electrical Characteristics. The C−V responses at room temperature with ac signal frequencies from 100 Hz to 1 MHz are shown in Figure 5. In comparison with the sample of HfO_2 on $In_{0.53}Ga_{0.47}As$, the frequency dispersion in the accumulation region was moderately improved after introducing an Al−O bond-incorporated passivation layer on the $In_{0.53}Ga_{0.47}As$ substrate, either by inserting an ultrathin Al_2O_3 passivation layer or by nanolaminating with Al_2O_3-starting atomic layers. This reduction of the frequency dispersion is believed to be closely associated with a smaller number of substrate element-related oxide bonds (especially, In and Ga according to the ToF-SIMS analysis) near the interface region.[23] For the $HfO_2/In_{0.53}Ga_{0.47}As$ sample, the capacitance has a largely increasing behavior in the inversion region, as shown in Figure 5(a), and this behavior indicates that the as-deposited C−V follows interface trap-responding characteristics rather than intrinsic inversion characteristics.[24,25] However, for the samples of HfO_2/Al_2O_3 and HfAlO on $In_{0.53}Ga_{0.47}As$, the inversion regime of the C−V curves in Figures 5(b) and 5(c) shows a response much closer to an intrinsic inversion at high frequency. This supports similar findings that reported that the insertion of an Al_2O_3 interlayer between HfO_2 and $In_{0.53}Ga_{0.47}As$ improves the high-frequency C−V characteristics.[8−10] Nevertheless, this still differs from a completely intrinsic inversion response and appears to have a partially interface-trap-assisted response, as the measurement frequency was decreased down to 100 Hz. Although the exact permittivity value of the dielectric stack could not be determined due to the frequency dispersion behavior, it can be noted that the accumulation capacitance values of the HfO_2/Al_2O_3 and HfAlO structures are quite close to each other. This implies that these two gate dielectric structures have a similar effective dielectric constant, considering their identical total physical thickness, and further justifies that a reasonable comparison of the electrical properties may be possible regardless of their net compositional difference.

In order to compare the interface trap density (D_{it}) among the samples, the capacitance (C_m) and conductance (G_m) were measured at different frequencies (f) in a parallel mode, and the equivalent parallel conductance (G_p) associated with the

interface traps was calculated without a series resistance correction using the following equation[26]

$$G_p = \frac{\omega^2 C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (2)$$

where ω is the angular frequency ($2\pi f$), and C_{ox} is the oxide capacitance. C_{ox} was assumed to be an accumulation capacitance measured at the lowest frequency (100 Hz), because of the difficulty in extracting the effective dielectric constant of the HfO_2/Al_2O_3 sample by thickness-series experiments. A two-dimensional plot of the normalized parallel conductance ($G_p/\omega qA$) as a function of gate voltage (V_g) and measurement frequency is shown in Figures 6(a)−(c). Here, q is the elementary charge, and A is the capacitor area. During the charge trapping and detrapping process via the interface states, the energy level of which is aligned with the Fermi level and maximum energy loss occurs at a certain frequency of the ac gate voltage. Therefore, the Fermi level movement can be traced from the normalized $(G_p/\omega qA)_{max}$ peak position along the frequency, which is closely related to the degree of Fermi level pinning.[27] For the $HfO_2/In_{0.53}Ga_{0.47}As$ sample, an identifiable $(G_p/\omega qA)_{max}$ peak at a given ac frequency was only found at a high frequency range, which implies that its movement with respect to the gate voltage is dominated by the Fermi level pinning or minority carrier response.[27] However, compared to the $HfO_2/In_{0.53}Ga_{0.47}As$ sample, both HfO_2/Al_2O_3 and HfAlO samples exhibited a steep change in frequency for a given gate bias range with distinctive $(G_p/\omega qA)_{max}$ peaks, which indicates more efficient movement of the Fermi level.

The D_{it} distribution in the upper region of the $In_{0.53}Ga_{0.47}As$ band gap was roughly estimated, as shown in Figure 6(d). The interface trap energy level (E_t) below the conduction band edge (E_c) was approximated using the following equation[28]

$$\Delta E = E_c - E_t = k_B T \times \ln\left(\frac{\upsilon_{th}\sigma N}{\omega}\right) \quad (3)$$

where k_B is the Boltzmann constant, T is the temperature, υ_{th} is the average electron thermal velocity, σ is the capture cross section, and N is the conduction band density of states. For the $In_{0.53}Ga_{0.47}As$ substrate, we used υ_{th}, σ, and N values of 5.6×10^7 cm s^{-1}, 1×10^{-16} cm^2, and 2.2×10^{17} cm^{-3}, respectively.[27] The D_{it} values were calculated by multiplying the measured $(G_p/\omega qA)_{max}$ values by 2.5 and were included in the graph only when the $C_{ox} > qD_{it}$ condition was satisfied.[27,28] It should be noted that the extracted D_{it} values may be slightly overestimated because the moderately underestimated C_{ox} was used (the accumulation capacitance measured at 100 Hz). However, when a proper C_{ox} value of the HfO_2 sample extracted from the thickness-series experiment was used, only a 10−15% decrease in the D_{it} values was observed. As shown in Figure 6(d), the $HfO_2/In_{0.53}Ga_{0.47}As$ sample has the highest D_{it}, while the stacked and nanolaminated samples had reduced values. The reduction of the D_{it} for the stacked and nanolaminated samples is believed to have been due to the existence of the Al_2O_3 passivation layer at the high-k/$In_{0.53}Ga_{0.47}As$ interface, as demonstrated in other studies.[8−10,13] The lowest D_{it} was achieved in the HfO_2/Al_2O_3 sample, probably due to the abundance of the Al−O bonds at the interface with much suppressed amount of the In and Ga-related oxides compared to the HfAlO sample, as revealed in the ToF-SIMS results [see Figures 2(b) and (c)].

In addition to the D_{it} characterization, the density of the near-interface slow traps that can electrically communicate with the underlying substrates, termed as "border traps,"[29] was compared among the samples by measuring the C−V hysteresis characteristics at 100 kHz with a sweep rate of ~0.16 V/s [Figure 7(a)]. The effective border trap density per unit energy

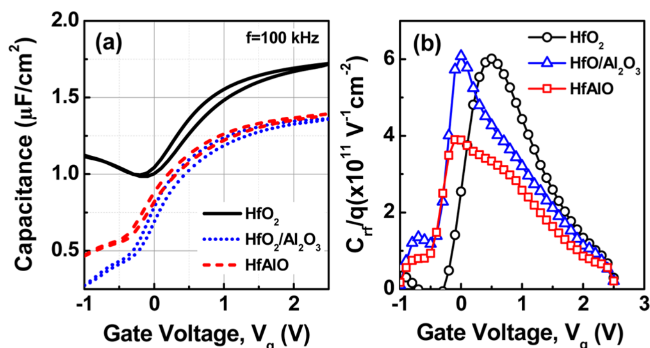

Figure 7. (a) C−V hysteresis characteristics and (b) effective border trap density per unit energy as a function of gate voltage for HfO_2, HfO_2/A_2O_3, and HfAlO gate dielectrics on $In_{0.53}Ga_{0.47}As$. The C−V measurement was performed at 100 kHz.

was calculated from the capacitance difference during the forward and reverse C−V scans [$C_{rf}(V_g) = |C_r - C_f|$] and is shown in Figure 7(b), where C_r and C_f are the capacitance densities at a given V_g during reverse and forward scans, respectively.[30] It reveals that the HfAlO sample has a smaller number of effective border traps than the HfO_2 and HfO_2/Al_2O_3 samples. It is known that the slow traps can be located at the interface region between the high-k film and the interfacial oxide (in our case, the interface between HfO_2 and Al_2O_3 in the stacked sample) or in the bulk of the high-k film (in our case, HfO_2, Al_2O_3, and HfAlO films) near the interface region with the substrate and can be measured from the hysteresis in C−V characteristics.[31] Therefore, it can be inferred that the distinctive interface between the HfO_2 and Al_2O_3 may act as electrically active border traps in a stacked structure, and the single-layered HfO_2 film has a greater number of bulk-related border traps than the Hf−Al−O mixed film due to the significant In/Ga diffusion into the high-k film.

We have employed a diverse set of I−V measurements to investigate the differences between the high-k dielectric structures on $In_{0.53}Ga_{0.47}As$ substrates. Figure 8 shows the I−V characteristics of the pristine samples under both gate and

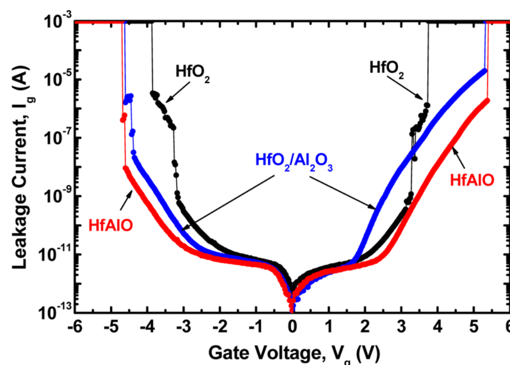

Figure 8. Leakage current characteristics of HfO_2, HfO_2/Al_2O_3, and HfAlO gate dielectrics on $In_{0.53}Ga_{0.47}As$.

substrate electron injection conditions. When the leakage current was compared roughly considering the flatband voltage difference, the most notable finding was that the HfO_2/Al_2O_3 sample exhibited a somewhat higher leakage current level than the HfAlO sample under substrate electron injection (positive gate bias). This is contradictory to the previously discussed result of the band structure estimation, showing the highest CBO of the HfO_2/Al_2O_3 structure with the $In_{0.53}Ga_{0.47}As$ substrate due to the ultrathin interfacial Al_2O_3 layer. However, because of the direct tunneling through the underlying ultrathin Al_2O_3 layer, the total leakage current of the stacked sample may be dominated by the overlying HfO_2 film. Furthermore, according to the border trap analysis, the stacked sample exhibited a higher border trap density than the nanolaminated sample, which might have contributed to the increase in the leakage current under substrate injection conditions. Among the three samples, HfAlO exhibited the most stable and lowest leakage current in both polarities, which can be understood by the increased band gap and CBO, as discussed in section 3.1. Park et al. reported that the electrical defects (oxygen vacancies) can be reduced by Al incorporation into HfO_2,[32] as proven in our border trap density measurement, which could be an additional factor for improving the leakage current characteristics of the nanolaminated structure compared to the stacked one with a similar accumulation capacitance.

For further comparison of the prepared dielectric structures, mainly with regard to the electrical stability under voltage stressing, two types of I−V measurement techniques have been employed under positive gate bias conditions, as shown in Figure 9: a consecutive forward/backward I−V measurement with different ending voltages (ramp voltages) under ramped-voltage stressing (RVS) and a transient current measurement (I-t) under constant-voltage stressing (CVS). During the RVS measurement in all the samples, the backward I−V curves were slightly shifted to a higher voltage region (with a decrease in the leakage current) in a reversible manner after low ramp-voltage stressing, which indicates that electron trapping in the gate stack occurs at a rather weak stressing condition.[33,34] A similar electron trapping behavior could also be found from the I-t characteristics shown in the inset of Figure 9, where the current continuously decreases as the time increases at a given gate voltage. These electron traps are known to originate from pre-existing traps rather than the newly generated defects (traps).[33,34] By raising the ramp voltage further, after a certain critical voltage, the backward I−V curve shifted in an opposite direction (to the lower voltage side), implying an increase in the leakage current, i.e., stress-induced leakage current (SILC), possibly due to the generation of new traps in the dielectric.[34] For the HfO_2 sample, new trap generation occurred at a ramp-voltage range of 3.4−3.7 V before the breakdown, which is much lower than the ranges of the HfO_2/Al_2O_3 and HfAlO sample, which were 4.4−5.2 V and 5.2−5.3 V, respectively, as shown in Figure 9. This suggests that the pure HfO_2 film is more vulnerable to voltage stress-induced breakdown and trap generation compared to the stacked or nanolaminated sample, which may have originated from the abundance of defective grain boundaries and/or In/Ga elements in the film (In−O bonds existing even in the bulk region of the film), as revealed by the TEM and ToF-SIMS analyses, respectively. Between the HfO_2/Al_2O_3 and HfAlO samples, HfAlO exhibited a minimal increase in SILC (due to lower trap generation), as shown in Figures 9(b) and 9(c), which could be due to the lower border trap density. Therefore, we can conclude that the HfAlO film has better long-term electrical stability compared to the HfO_2/Al_2O_3 film on the $In_{0.53}Ga_{0.47}As$ substrate.

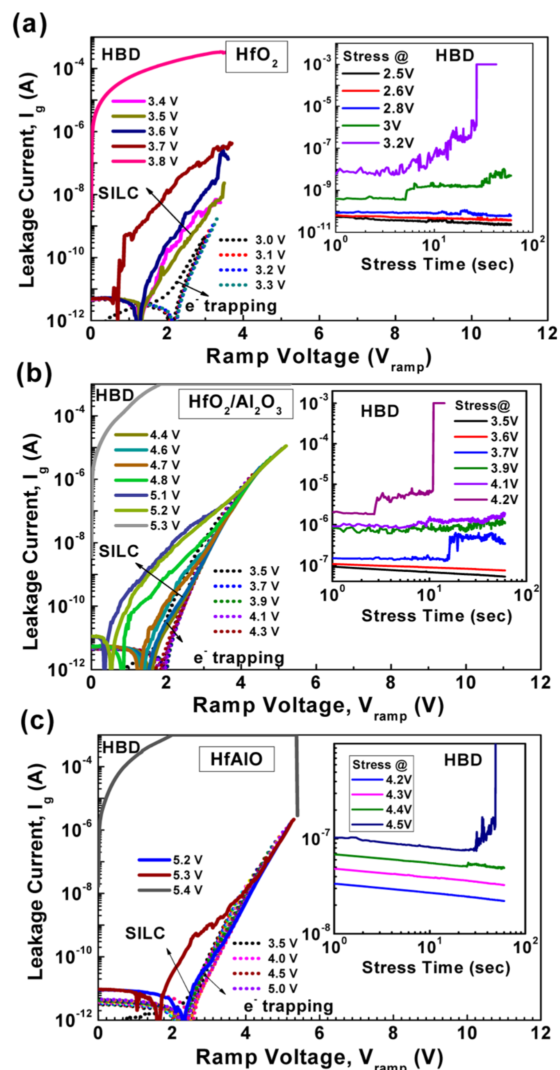

Figure 9. Leakage current vs ramp-voltage characteristics of (a) HfO_2, (b) HfO_2/A_2O_3, and (c) HfAlO gate dielectrics on $In_{0.53}Ga_{0.47}As$. Dotted lines show electron trapping behavior and solid lines represent SILC characteristics under different increasing end voltages. Insets show the transient current characteristics (I-t) for each gate stack.

4. CONCLUSION

Detailed electrical analyses of ALD-based HfO_2/Al_2O_3 (stacked) and HfAlO (nanolaminated) high-*k* structures on $In_{0.53}Ga_{0.47}As$ with a similar accumulation capacitance were performed. From SIMS measurement, more suppression of In out-diffusion was confirmed using stacked or nanolaminated structures with an Al−O-related passivation layer on the $In_{0.53}Ga_{0.47}As$ substrate as compared to the HfO_2-only structure. In the case of the HfAlO film, the band offsets and band gap had a monotonically varying trend between the pure HfO_2 and Al_2O_3 films, according to the band structure analysis. The Al−O-related passivation layer on the $In_{0.53}Ga_{0.47}As$ substrate enabled more efficient movement of the Fermi level and reduced the interface state density, compared to the single-layered HfO_2 structure. Although the interface state density of the nanolaminated structure seems to be slightly higher than that of the stacked structure and requires further optimization, a

lower border trap density, lower leakage current, and better SILC characteristics under substrate electron injecting RVS/CVS conditions were observed than in the HfO_2/Al_2O_3 structure at a similar capacitance-equivalent oxide thickness.

■ ASSOCIATED CONTENT

Supporting Information

Detailed ALD parameters for the preparation of different dielectric structures and additional TEM analysis results for the as-deposited and annealed samples. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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